# Biscayne™

PRODUCT BRIEF

## OVERVIEW

Biscayne, a member of Bay Microsystems' Internetworking Processor™ (InP) Family, is a Classification Processor with Policing that can be programmed to parse, classify and police packets and cells at rates of up to 16 Gbps, at minimum packet size with any traffic pattern. Biscayne connects seamlessly to Bay's other InP™ Family members, including Montego, a single chip OC192c/10G programmable Internetworking Processor, Traffic Manager and SAR.

**Performance**: Supporting applications from "Access to Long Haul", Biscayne is today's highest performance classification processor with policing, whether used in low cost enterprise networks or in high performance core networks.

- *Packet Search Rate: > 400 million searches/sec*
- *Packet Processing Rate: 41.5 million packets/sec*
- *Ingress/Egress Data Rate: 16/16 Gbps*

**Service Breadth**: Biscayne's classification supports existing and emerging services, including IPv4, IPv6, ATM, POS, Ethernet, Frame Relay, MPLS and DiffServ, thus preserving investments in legacy equipment while enabling new profitable services.

Biscayne's policing, the first of its kind, supports flexible algorithms required for sophisticated DiffServ, Ethernet, Frame Relay and ATM. It augments and enhances the classification and policing capabilities of a downstream NPU/TM, and provides a direct interface between the two devices. Network systems OEMs can now accomplish more complex tunnel resolution and routing for such products as multi-protocol edge routers and voice/wireless gateways. Biscayne can classify extra long headers; multiple labels; and highly complex, deeply embedded multi-field headers.

**Interfaces**: Biscayne interfaces to any SPI-4.1/SPI-4.2/ SPI-3 compliant processors, MACs and framers, thus supports OC48 and OC192c/10G applications. It supports flexible packet parsing and key generation with direct interfaces to TCAM and SRAM search memories.

**Simplified Programming Model**: Bay's NEXTware™ software programming environment uses easy to configure ANSI C API functions and a cycle/pipeline accurate C-simulator to capitalize on the simplified programming model to quickly apply, verify, and debug applications for any traffic pattern and network service.

**Internetworking Development System (IDS)**: Bay's IDS minimizes learning and development time by providing a complete OEM application ready system, hardware emulation platform, software simulation platform and reference design. It is available today and includes Java GUIs, CLI, NEXTware™ API, System Administration Server (SAS), Intermodule Communication, Vxworks OS, Board Support Package (BSP), diagnostics, TCP/IP stack and drivers.

## FEATURES

**Deterministic, Scalable Architecture**: Superscalar, pipelined architecture tackles non-deterministic traffic patterns.

**Targeted Applications**

- Native Ethernet – IEEE Bridge/switch, VLAN forwarding, VLAN port and protocol classification
- IETF PPVPN – VPLS, L2VPN
- IETF PWE3 – ATM and Ethernet PE tunneling
- MPLS – Label Edge Routing (LER), Label Switch Routing (LSR), VLAN to MPLS mapping
- Legacy UNI – Frame Relay and ATM
- IPv4 – Forwarding and Routing
- IPv6 – Tunnel resolution and Forwarding

**Searching**

- > 400 million searches/sec with programmable key generation
- Up to 14 searches per packet at OC192c without statistical multiplexing
- Price points and table sizes scale for the application with no performance penalty: up to 8M routes and 1M labels

**Classification, Parsing and Tagging**

- Flexible support for standard, proprietary and future protocols
  - IPv4, IPv6, ATM, FR, PPP
  - MAC, VLAN, L2TP, MPLS, DiffServ, Traffic Engineering
  - ACL, System Rules
  - Direct and indirect searches
- Full external context memory support
- Header popping for tunnel termination: fully supports chaining for complex tunnel resolution
- Fast path MAC learning and aging, and spanning tree support
- Per rule filtering
- Editing and tagging

**Policing and Statistics**

- DiffServ, Frame Relay, Ethernet and ATM support
- Dual leaky bucket, token bucket and Committed-Max-Excessive policing algorithm support
- Flow based and trunk based policing
- Metering, marking and QoS internetworking
- Up to 1 million 36-bit counts for per-flow packet/byte statistics

**Physical Specifications**

- SPI-4.2, SPI-4.1 and SPI-3 compliant interfaces
- 1156 pin FCBGA
- 0.15mm CMOS process
- 4W at 5Gbps ingress and egress data rate
- 5W at 10Gbps ingress and egress data rate
- 6W at 16Gbps ingress and egress data rate


Internetworking Intelligence Performance

Deterministic Scalable